NITRIDE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The disclosure of Japanese Patent Application No. 2007-318058 filed in Japan on Dec. 10, 2007 including specification, drawings and claims is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to nitride semiconductor devices and method for fabricating the nitride semiconductor devices, and particularly relates to a power transistor for use in, for example, a power supply circuit and a method for fabricating the power transistor.

[0003] In recent years, field effect transistors (FETs) made of gallium nitride (GaN)-based semiconductors have been intensively studied as high-frequency high-power devices. III-V nitride semiconductors such as GaN form various types of mixed crystal together with aluminum nitride (AlN) and indium nitride (InN). Thus, GaN-based semiconductors form heterojunctions in the same manner as conventionally-used arsenic-based semiconductors such as gallium arsenide (GaAs).

[0004] In particular, a heterojunction of a nitride semiconductor has a characteristic in which spontaneous polarization and/or piezoelectric polarization produces a high concentration of carriers at the interface thereof even when the nitride semiconductor is not doped. As a result, FETs using nitride semiconductors are likely to exhibit depletion-mode (normally-on) characteristics, and thus it is difficult to obtain enhancement-mode (normally-off) characteristics. However, most of the devices currently used in the power electronics market are normally-off devices, and normally-off operation is also strongly demanded for FETs using GaN-based semiconductors.

[0005] Normally-off FETs are implemented with, for example, a structure in which a gate region is recessed so that the threshold voltage is positively shifted (see, for example, T. Kawasaki et al., "Solid State Devices and Materials 2005 tech. digest", 2005, p. 206). A method with which a FET is fabricated on the (10-12) plane of a sapphire substrate so that no polarization electric field is generated in the crystal growth direction of nitride semiconductor (see, for example, M. Kuroda et al., "Solid State Devices and Materials 2005 tech. digest", 2005, p. 470) is also known. In addition, as a promising structure for obtaining a normally-off FET, a junction field effect transistor (JFET) in which a p-type GaN layer is formed as gate is proposed (see, for example, Japanese Laid-Open Patent Publication No. 2005-244072). In a JFET structure, piezoelectric polarization produced at the heterointerface between a channel layer of undoped GaN and a barrier layer of AlGaN is canceled by piezoelectric polarization produced at the heterointerface between the barrier layer of AlGaN and a p-type GaN layer. This structure reduces the concentration of two-dimensional electron gas immediately under a gate region where the p-type GaN layer is formed, thus obtaining normally-off characteristics. The use of a pn junction having a larger built-in potential than that of a Schottky junction for gate advantageously reduces gate leakage current even with an application of a positive gate voltage.

SUMMARY OF THE INVENTION

[0006] The present inventors actually fabricated the conventional JFET described above to find the problem of occurrence of so-called current collapse. Specifically, when the gate is switched from OFF to ON immediately after an application of a high drain voltage, drain current decreases and the ON resistance increases, as compared to the case where lower drain voltage is applied. The increase in ON resistance due to the current collapse is a serious problem in power transistors to which high drain voltages are applied.

[0007] It is therefore an object of the present invention to suppress occurrence of current collapse to implement a normally-off nitride semiconductor device applicable to a power transistor.

[0008] To achieve the object, a nitride semiconductor device according to the present invention has a structure in which a nitride semiconductor layer having a gate recess is formed on a nitride semiconductor layer forming a heterojunction interface and a p-type semiconductor layer is formed in the gate recess.

[0009] Specifically, a nitride semiconductor device according to the present invention includes: a substrate; a first nitride semiconductor layer formed on the substrate; a second nitride semiconductor layer formed on the first nitride semiconductor layer and having a band gap energy larger than that of the first nitride semiconductor layer; a third nitride semiconductor layer formed on the second nitride semiconductor layer and having an opening; a p-type fourth nitride semiconductor layer filling the opening; and a gate electrode formed on the fourth nitride semiconductor layer.

[0010] In the inventive nitride semiconductor device, a channel layer formed between the first nitride semiconductor layer and the second semiconductor layer is kept away from the surface. Accordingly, unlike a conventional nitride semiconductor device, a noticeable advantage in which the influence of the surface state on the channel layer is reduced and occurrence of current collapse resulting from the surface state is suppressed is obtained. In addition, since the second and third nitride semiconductor layers are both made of nitride semiconductor, these layers are allowed to be continuously grown. Accordingly, no interface state is formed in the interface between the second nitride semiconductor layer and the third nitride semiconductor layer so that the influence of the interface between the second and third nitride semiconductor layers does not need to be taken into consideration. With this structure, occurrence of current collapse is more effectively suppressed. Moreover, since the gate electrode is formed on the p-type fourth nitride semiconductor layer, the concentration of two-dimensional electron gas immediately under the gate electrode is selectively lower than that in the other region. As a result, normally-off characteristics are obtained. It is also possible to increase the range of the threshold voltage, thus implementing a threshold voltage of about +1V.

[0011] A method for fabricating a nitride semiconductor device includes the steps of: (a) epitaxially growing a first nitride semiconductor layer, a second nitride semiconductor layer having a band gap energy larger than that of the first nitride semiconductor layer and a third nitride semiconductor layer in sequence over a substrate; (b) selectively removing the third nitride semiconductor layer to form an opening; (c) epitaxially growing a p-type fourth nitride semiconductor